A HIGH POWER FACTOR AC-TO-DC CONVERTER FOR DISTRIBUTED POWER SYSTEMS

Michael Elmore and Steve Newton
IBM Power Systems
IBM Corporation, Endicott, New York 13760

Abstract

An AC-to-DC converter, which achieves high power factor and low current distortion in conformance with IEC-555-2, is presented. A boost, with zero-current switching at turn-on and zero-voltage switching at turn-off, is cascaded with an unmodulated, zero-voltage switched half-bridge to achieve high efficiency. Unique packaging technology gives excellent thermal performance for increased reliability.

Introduction

The number of strategies for achieving high power factor and low current distortion in off-line power applications has surged in recent years. Mammano and Dixon (1) have outlined the benefits and disadvantages of each of the major topologies: boost, buck and buck-boost. Other topologies exist, such as the sepic (2) and resonant (3) converters, but by far the most popular topology has been the boost converter.

The boost converter offers many advantages over other topologies. Probably the single most important advantage is the possibility of continuous input current. This allows a smaller input filter to be used, which saves on the size and cost of the complete system. The boost converter also switches from 0 to the peak of the input AC line. This allows current to be drawn during the entire cycle of the input. If the boost output voltage is set at about 400VDC, no range switching of the input is required and operation from 85VAC to 265VAC is possible. The high voltage on the output also results in longer hold-up times for less bulk capacitance. With the boost topology, power factors of greater than 99.9% and input current distortions of less than 3% have been reported (7).

The boost topology itself offers may different inplementations to yield high power factor and low current distortion. Barabas (5) uses a conventional current mode integrated control circuit (UC3842) and limits the bandwidth to achieve high power factor. The current draw is in the shape of trapezoids. Input current total harmonic distortion (THD) is typically about 12% or higher. Peterson (6) boosts during the beginning and end of each line half-cycle, while operating in a passive mode during the middle portion of the line half-cycle. This approach is a compromise between purely passive filtering and active power factor correction. It achieves very high efficiency and an output voltage that is less than the peak of the input AC line, but the power factor is only about 96%, while THD is around 19%.

More conventional control schemes exist to give very high power factor and low THD. Usually, peak switch current is compared to a reference that is the product of the rectified input AC line and an output voltage error signal (7). This is classical current mode control. Mammano (1) also uses a sinusoidal reference derived from the AC line, but with average current mode control. The advantage of these control techniques is that the boost may be operated in the continuous mode and at a constant frequency. It is even possible to use a hysteretic control to keep the boost in the continuous mode (4).

While continuous mode operation with current mode control is very attractive, it is not without its drawbacks. Diode reverse recovery stress, provides a practical limit to the frequency of operation, output voltage level and converted power. Switching losses can also be a concern. It is for these reasons that the boost is sometimes run in discontinuous mode. Operating in the discontinuous mode gives peak switch currents that are more than twice as high as in continuous mode operation, but diode reverse recovery current is zero. Switching losses are less than in continuous mode, although conductive losses are higher. However, the peak switch current can be kept to only twice the input current, if the boost is controlled to operate on the boundary between continuous and discontinuous mode, as shown in Figure 1.

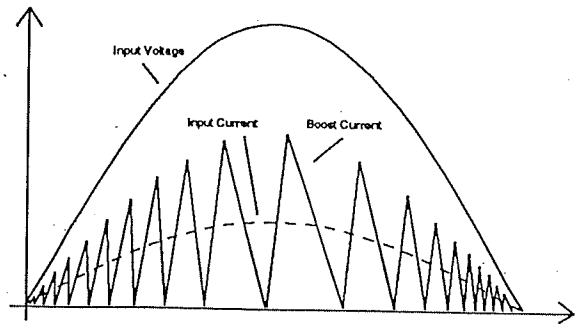

Figure 1. Boost Current on Boundary Between Continuous and Discontinuous Mode

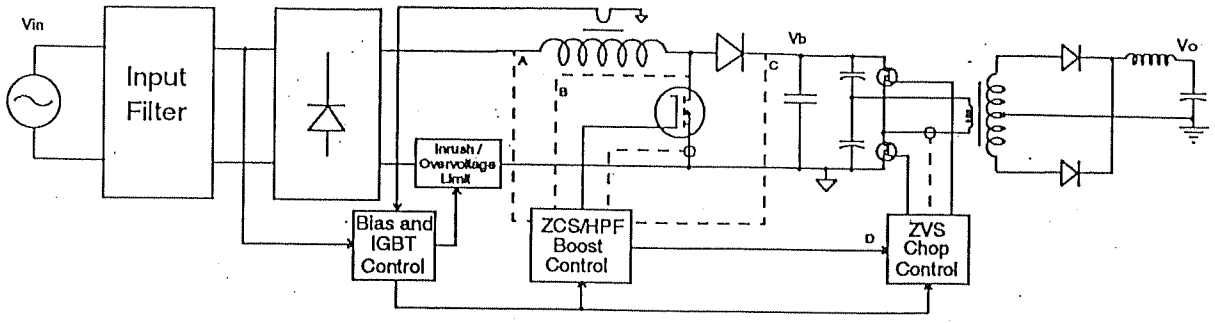

Figure 2. Block Diagram of Boost-Chop Distributed Power System

This kind of control results in variable frequency switching. The frequency is higher at light loads and higher input voltages. The current through the boost inductor is near zero at turn-on. There is no ringing on the switch drain at turn-off, so no snubber is needed to control noise. The only real disadvantage of this mode of operation is that a large input filter is required to smooth the input current. Hall (8) has reported good results with this technique.

While the critically continuous, power factor corrected boost converter manages to convert off-line AC voltage to a high voltage DC bus, it does not provide the required isolation. Isolation is needed to meet safety standards and prevent circulating currents. Isolation can be provided at the point of regulation by individual DC-to-DC converters. With this architecture the primary side referenced boost output is distributed around the system. A DC-to-DC converter with isolation is located at each point in the system, where a regulated, secondary side voltage is required. Currents are prevented from circulating around the system, because of the local isolation. However, this kind of system must deal with a primary side referenced, distributed high voltage. This can complicate system design, because of the safety issues involved.

Another approach is taken here. Input-to-output isolation is done once, only at the boost output stage. Also, the high voltage boost output is reduced to a low voltage. The distributed voltage is now secondary side referenced and is a low voltage (24VDC - 48VDC). The high voltages associated with the primary can now be confined to a central location, simplifying overall system design. Current loops can be avoided with careful attention to system layout.

While many topologies are available to implement the isolation stage of the power system, a zero voltage switched half-bridge is an attractive solution. This is a conventional half-bridge with each switch operating at near 50% duty cycle. There is no output voltage feedback. The converter is essentially a DC-to-DC transformer. The cascaded boost and unmodulated, half-bridge converters are referred to as a boost/chop converter.

System Description

Figure 2 shows a block diagram of the boost-chop distributed power system. Between the AC line input and the bridge rectifier is a filter. The filter averages the boost inductor current to produce a smooth input current as shown in Figure 1. The magnitude of the peak of the input current is one-half the magnitude of the peak inductor current. The input filter also eliminates emissions conducted to the power line. A resistor in series with the boost inductor provides inrush current limiting. When the boost starts to switch, a tap on the boost inductor provides gate drive to an IGBT, which shorts out the inrush resistor. The boost is held off unless the AC input line is above 73 Vrms. The bias supply becomes active at an even lower line voltage, thus insuring that no race problems occur at start-up. After the initial inrush of current, the boost soft-starts to bring the boost output, or bulk voltage, Vb, to 400 VDC. When the bulk voltage reaches about 360 VDC, the chop converter is turned on by a command (D in Figure 2) from the boost control. The chop also soft-starts to bring the output voltage to its steady-state value in a linear fashion without overshoot.

The boost and chop converters both have overcurrent limiting. The boost shuts down in the event of an overvoltage on the bulk voltage. A long duration overvoltage transient on the AC input line also shuts down the boost and opens the IGBT. This puts the inrush current limiting resistor in series with the AC line voltage and limits charging of the bulk capacitor. The chop converter continues to deliver power to the output during the overvoltage. Short duration overvoltage transients are attenuated with a clamp in the input filter stage.

The boost control and power MOSFETs are mounted on an IBM proprietary thermal carrier. The control consists of a custom integrated circuit, jointly developed by IBM Power Systems and Harris Corporation of Melbourne, Florida, and external SMT passive components. The external components are used for high voltage sensing and add design flexibility to the module, since they are easily modified. Figure 3 shows the boost module.

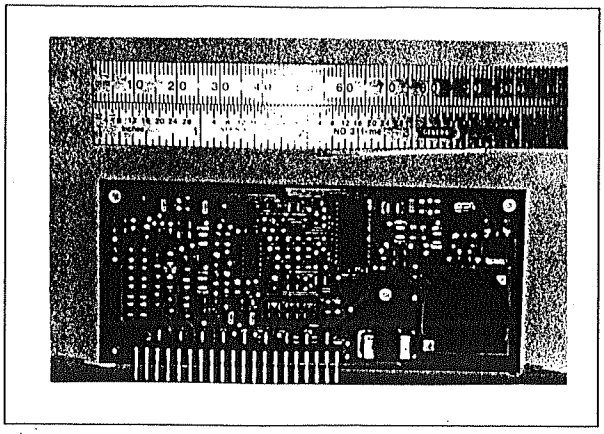

Figure 3. Boost Module

The chop control module is a mixed, pin and through hole and SMT circuit card. It generates a high-side and low-side drive for two power MOSFETs that are the switches for the chop converter. The chop control also senses chop primary current for overcurrent limiting and short circuit protection.

The bias and IGBT control module provides two functions for the boost/chop power system. It generates two 12VDC supplies to power the boost and chop modules. It also controls the turn-on and turn-off of the IGBT through the tap winding on the boost inductor. This module is also a mixed, pin and through hole and SMT circuit card. Figure 4 shows the chop and bias and IGBT control modules.

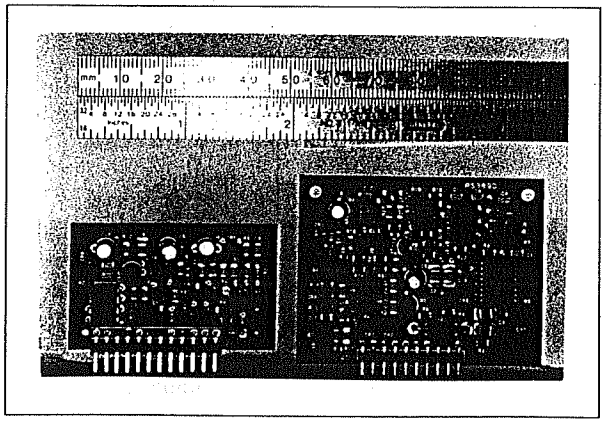

Figure 4. Chop and IGBT Control Modules. The chop control module is on the right.

Boost Circuit Operation

The boost switches at the boundary between continuous and discontinuous mode. This critically continuous mode of operation insures that switch turn-on losses are minimized. Figure 5 shows idealized switch voltage and inductor current waveforms. The on-time of the switch is set by the boost control integrated circuit to provide the required energy to the load. The switch off-time begins at A. During the off-time, inductor current flows into the bulk capacitor and through the chop to the load. When the inductor current falls to zero at B, the switch drain voltage begins to fall from its clamped value, Vb. Energy stored in the parasitic switch capacitance, Cp, now starts to flow back through the inductor and into capacitance, Cin, located across the input rectifier. The current in the inductor reaches its negative maximum value at C, when the voltage on the drain equals Vin, i.e., when the voltage across the inductor is zero. The drain voltage continues to fall towards its minimum value, as the inductor current increases from its maximum negative value to zero again. When the drain voltage reaches its minimum value at D, the inductor current is zero and the switch turns on. The boost control IC senses the drain voltage level to turn on the switch.

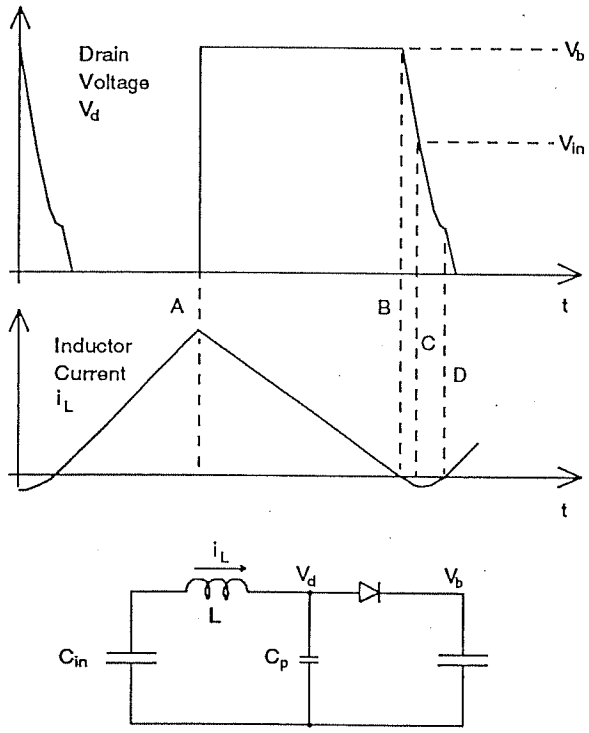

Figure 5. Idealized Boost Waveforms

A simplified circuit diagram of the boost module is given in Figure 6. Inputs and outputs, labeled A, B, C, and D, reference the same labeled points in Figure 2.

The boost control integrated circuit is M1. DRAIN and DDREF are compared to determine when the drain of Q2 has reached its minimum value, D, in Figure 5. Equal voltages on DRAIN and DDREF indicate zero voltage across the boost inductor. However, R25 and C11 add a small delay, so that the on-time does not start until the drain voltage has rung to its minimum value. INRMS monitors the rectified AC input and is used to adjust the boost gain with variations in line voltage. This guarantees good line and load transient response over the full universal input range. C17 and the error voltage set the on-time. C17 will impose a limit on the

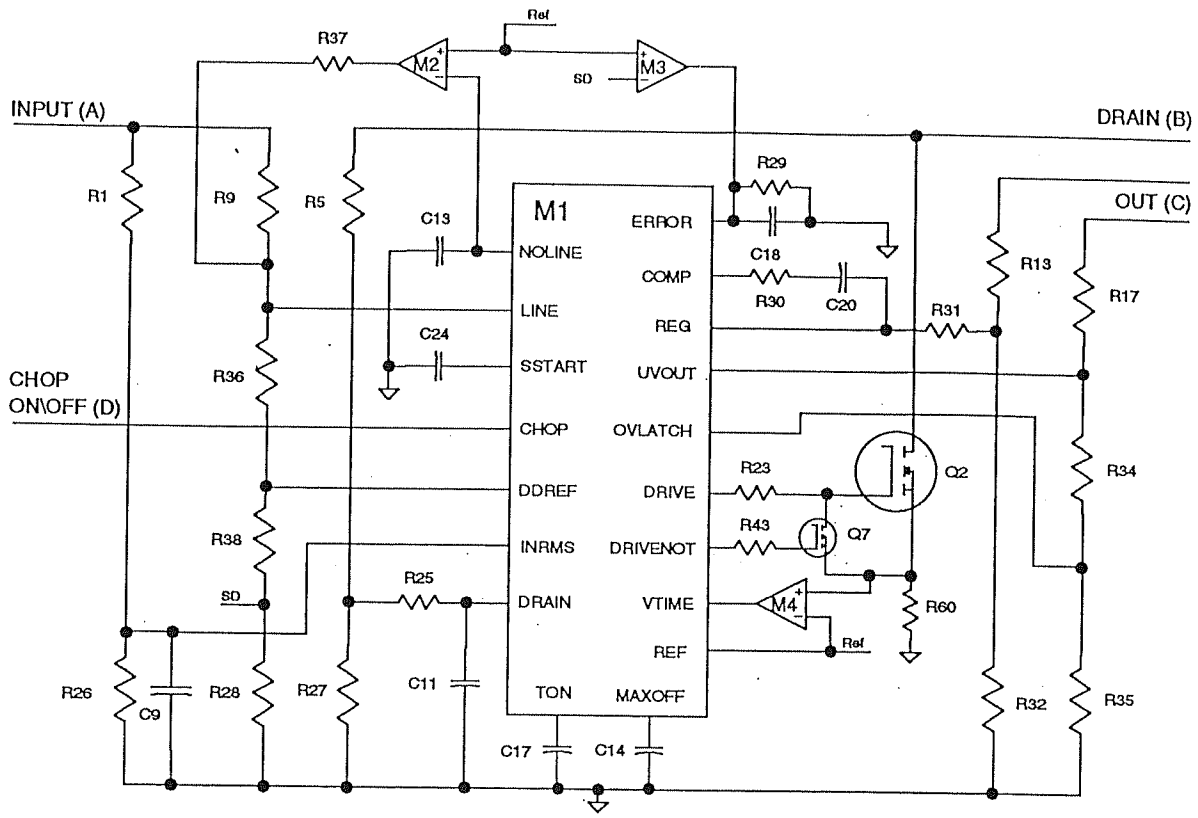

Figure 6. Simplified Circuit Diagram of the Boost Module

amount of energy that can be delivered to the load at low-line. C14 sets the maximum allowable off-time. This insures that switching will always occur, even at the peak of the AC input at high line. Under this condition, the voltage across the inductor during the off-time may be small enough that noise could confuse the normal DRAIN and DDREF compare operation. MAXOFF guarantees that the next on-time will start.

LINE and NOLINE are used for AC input under-voltage lockout and AC input overvoltage shutdown. At start-up C13 is charged to 5.1V and the output of comparator M2 is low. When the AC input goes above 73Vrms, C13 is discharged and the boost starts to switch. At the same time the output of M2 goes high. C13 starts to recharge at a linear rate and continues to charge during that portion of the cycle that the AC input is below 62V. However, so long as the AC input stays above 73Vrms, C13 does not have time to recharge to 5.1V between half-cycles of the AC input and the boost stays on. The AC line must fall below 62Vrms to turn off the the boost. If the AC input goes above 265Vrms, this is detected at SD. off. The boost is turned off by comparator M3. M3 pulls ERROR, the boost control error voltage, low. As soon as the AC input falls below 265Vrms, the boost starts to switch again. C24 sets the boost soft-start on-time.

The boost output voltage is sensed by R13 and R32 for regulation. Loop gain is adjusted with R31 to precisely set the closed-loop gain at 15Hz. The loop is compensated by changing the values of R30, R31, and C20. R17, R34, and R35 monitor the boost output voltage for overvoltage and undervoltage conditions. Until the boost output reaches 360V, the CHOP output is held low. CHOP is used to turn the chop converter on and off. If the boost output should climb to 450V, the boost is latched off. Input power must be cycled to restart the boost. Current in Q2 is monitored by a resistor, R60, in its source. If current exceeds a predetermined level, comparator M4 terminates the on-time.

Chop Circuit Operation

Figure 7 shows waveforms for a modulated half-bridge circuit. High-side and low-side drivers turn on each switch in the half-bridge for an amount of time necessary to set the output voltage. This closed-loop system results in tight output regulation and fast transient response. Turn-on losses can be high though. When the high-side switch turns on at E, it has one-half the bulk voltage, Vb, across it. The same is true of the low-side switch. This would be 200 VDC in the boost-chop system presented here. Considerable noise is also generated during turn-off by parasitic ringing of transformer magnetizing and leakage inductances with switch and other circuit capacitances. When the low-side switch turns off at A, it is clamped to the bulk voltage, Vb, at B. When the high-side switch turns off at C, the voltage is clamped to ground at D.

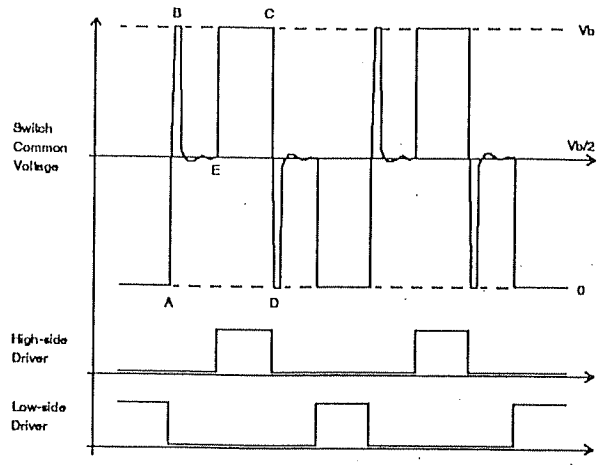

Figure 7. Modulated Chop Switch and Driver Waveforms

If, on the other hand, the high-side switch is turned on at B, both problems associated with the modulated half-bridge are avoided. Energy stored in the transformer magnetizing and leakage inductance has driven the voltage across the low-side switch high, where it has been clamped at the bulk voltage, Vb. The high-side switch is turned on before the voltage starts to ring low. Consequently, the high-side switch turns on with near zero volts across it and switching losses are zero. Similarly, the low-side switch is turned on at D, yielding zero voltage switching. This is illustrated in Figure 8.

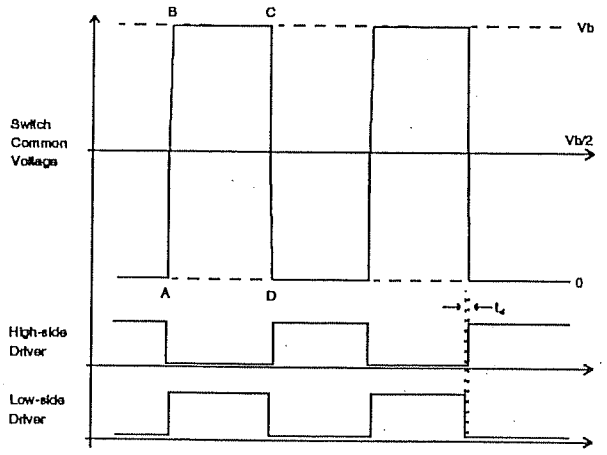

Figure 8. Unmodulated Chop Switch and Driver Waveforms

The unmodulated half-bridge or chop, as it is referred to here, cannot operate each switch at 50% duty cycle. There must be a small amount of time after one switch turns off and before the other switch turns on. This dead-time, td, is shown in Figure 8. The dead-time is about 200ns and prevents simultaneous conduction of both switches, which would result in their failure.

During start-up, the chop duty cycle is slowly increased from 0 to just under 50%. Switch waveforms, like those in Figure 7, will occur during start-up. Once the chop reaches steady-state operation switch modulation cannot occur. Load regulation will be a function of drops in the chop power train. These drops come from printed wiring board and external wiring resistive losses and secondary side diode and primary side switch losses. Drops due to leakage inductance also place a pratical limit on chop switch frequency. However, load regulation in the system is still acceptable. DC-to-DC converters, which operate from the output, regulate out any change in distributed voltage. A block diagram for the chop control module is shown in Figure 9. Since the clock and PWM circuits use high speed CMOS logic, the chop VCC from the bias module is regulated down to 5VDC. The high voltage bridge driver is a IR2110. It generates the high-side and low-side drive for the chop MOSFETs.

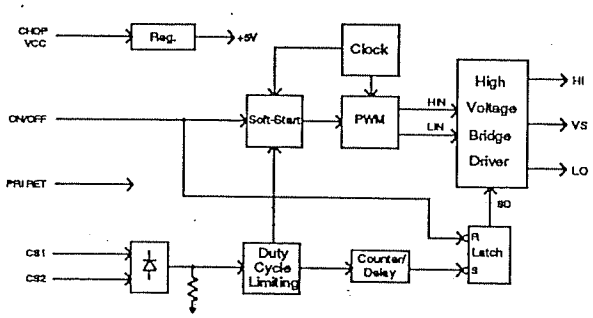

Figure 9. Block Diagram of Chop Control Module

Primary side current is sensed with a current sense transformer and rectified on the control module. In the event of an output short circuit or overcurrent condition the chop duty cycle is cut back. The chop essentially becomes a current source, until a built-in delay latches the chop off. The on/off input must be cycled low to high to restart the chop. This only occurs, if the AC line voltage is recycled.

Bias and IGBT Control Operation

The bias supplies for the boost and chop converters and the control for the IGBT are both located on the same module, as shown in Figure 4. The block diagram for the module is given in Figure 10.

The bias supplies use an HV2405 AC-to-DC converter integrated circuit made by Harris Corporation to provide a +12VDC output to power the chop converter. This circuit is a two stage converter. The front end of the IC converts the AC line voltage to an 18VDC bulk voltage. The back end of the IC is a linear regulator that converts the 18VDC bulk to 12VDC. An independent linear regulator converts the 18VDC bulk to a second 12VDC output to power the boost converter. The second regulator is required to limit noise interactions between the boost and chop. Once the chop

converter comes into regulation, a bias winding on the chop transformer inhibits the HV2405 front end. Power for both the chop and boost converters is now supplied from the chop bias winding. If the chop should shut down, due to a fault, the front end of the HV2405 will supply power to the boost and chop converters again.

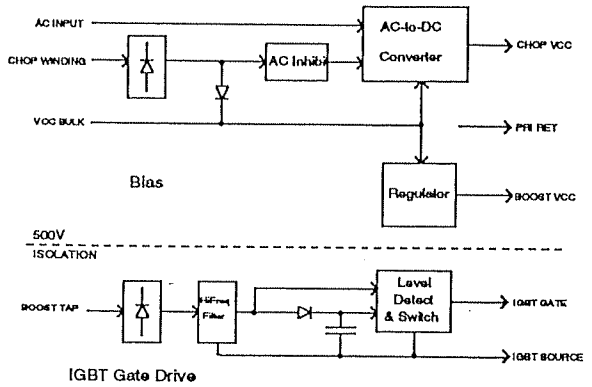

Figure 10. Block Diagram of Bias and IGBT Control Circuits

The IGBT gate is driven from a tap on the boost inductor. The tap winding voltage is rectified and passed through a high frequency filter to produce a wavefrom that resembles the fullwave rectified AC line voltage. This filtered waveform serves two purposes: (1) It charges a capacitor, C2 in Figure 10, to provide a 15V bias for the IGBT gate. And (2) it provides a signal to turn off the IGBT during a fault, such as a high voltage AC line transient. The boost control module monitors the AC line voltage and turns the boost off if the input voltage climbs above 380V peak. As soon as the boost stops switching, the voltage on the boost inductor tap winding goes to zero. The IGBT control module senses this and turns off the IGBT. C2 has sufficient stored energy to power the IGBT control module during turn-off, even though the boost tap winding has zero volts on it. As a consequence of this turn-off control scheme, the IGBT can be gated off during zero crossing of the AC line voltage. This action is acceptable though, since little or no current is drawn from the source near zero crossing. Figure 11 shows the IGBT gate voltage and its relationship to the rectified AC line voltage.

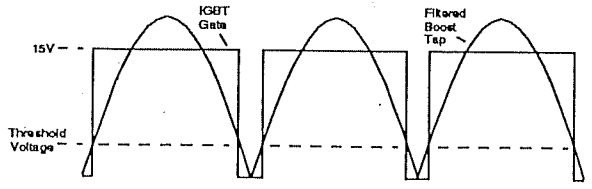

Figure 11. IGBT Control Waveforms. The filtered, rectified boost tap winding voltage is idealized for clarity. The actual waveform is nearly trapezoidal and has a high frequency component at the boost switch frequency.

Circuit Analysis

Since the ZCS boost PFC operates with a variable frequency, it is necessary to deal with average quantities for most practical design work. The ZVS chop is more straight forward, since it operates at a fixed frequency. Only the boost is considered here.

Boost Design Equations

An expression for average frequency allows the designer to pick an inductor that will result in acceptable switching losses and peak currents and minimize the input AC line filter size. The average power drawn by the boost over one AC input period, T_L is

$$P_{in} = \frac{1}{T_L}\int_0^{T_L} v(t)i(t)dt \qquad (1)$$

where $v(t)$ and $i(t)$ are the instantaneous AC input voltage and current, respectively. Assuming the boost switch on-time, $T_{on} << T_L$, the instantaneous average input current is given by

$$i(t) = \frac{1}{2} I_L(t) = \frac{1}{2}\left(\frac{v(t)T_{on}}{L}\right) \qquad (2)$$

where $I_L(t)$ is the peak inductor current at the end of T_{on}. Substituting equation (2) into (1) with $v(t) = \sqrt{V_{rms}}\ \sin(t)$ and solving for T_{on}, gives

$$T_{on} = \frac{2P_{in}L}{V^2_{rms}} \qquad (3)$$

T_{on} is constant over T_L. The boost switch off-time, $T_{off}(t)$, is

$$T_{off}(t) = \frac{LI_L(t)}{V_o - V(t)} \qquad (4)$$

which is not constant over T_L. Since the instantaneous period, $T(t) = T_{on} + T_{off}(t)$, the instantaneous frequency, f(t), is

$$f(t) = \frac{V_o - V(t)}{T_{on}V_o} \qquad (5)$$

To obtain the average switch frequency over one cycle equation (5) is integrated over one cycle with $v(t) = \sqrt{2}\ V_{rms}\sin(t)$. The result is

$$f_{avg} = \frac{2P_{in}L}{V^2_{rms}}\left[1 - \frac{2\sqrt{2}}{\pi}\frac{V_{rms}}{V_o}\right] \qquad (6)$$

Generally, the boost inductor is chosen to give an average switch frequency of 100kHz at nominal line and load. However, the effects of extreme line and load on average frequency must be investigated. Very light load will send the boost into a burst mode. Care must be taken to insure that IEC-555-2 is still met under this condition.

Test Results

A 600W version of the boost-chop distributed power system was built and tested for performance. Table 1 shows the major circuit component values used. The system was tested at room temperature in an open frame with a fan blowing air over it. Figure 12 shows AC line input current. There is a small amount of distortion near zero crossing, because the low input voltage does not ramp current up enough in the boost inductor during T_{on} to offset the resonant current shown in Figure 1.

Power factor is plotted as a function of load for three AC line voltage values in Figure 13. Power factor improves with increases in AC input current. This is not surprising, because of the zero crossing distortion mentioned previously. AC input current distortion is compared against the IEC-555-2 standard in Figure 14 for the first fifteen harmonics of the 60Hz fundamental line frequency. The boost-chop system comfortably meets and exceeds the standard at each harmonic. THD is 8.8%.

Efficiency is plotted in Figure 15. Since not all the component values listed in Table 1 were optimized, the efficiencies are a little lower than calculated values. It is expected that efficiencies will run between 87% and 92%, with loads between 200W and 600W, in a fully optimized design. For the same reason, the load regulation shown in Figure 16 is a little looser than expected, but still about ±5% from 3A to 19A output current.

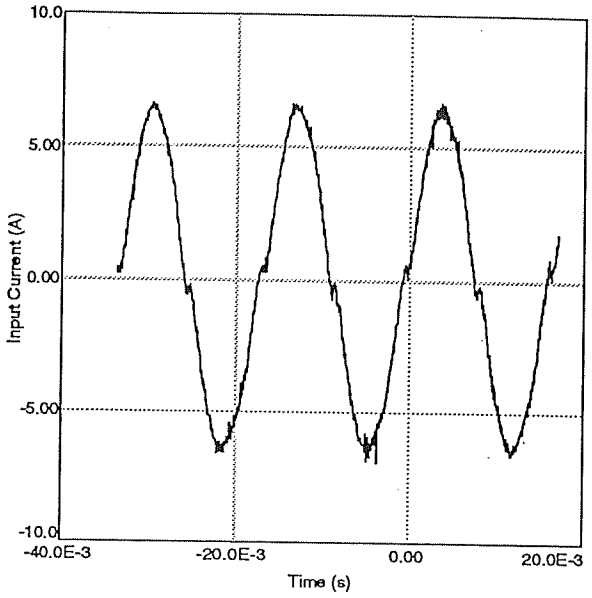

Figure 12. AC Line Current. V_{in} = 180V_{rms} and P_{load} = 600W

Figure 17 shows the start-up of the boost output voltage in response to a step input of 120V_{rms}. Once the inrush portion of the start-up sequence has been completed, the output voltage increases linearly to 400VDC. This linear ramp is the boost soft-start portion of the start-up sequence. The total time for start-up can be adjusted to fit a particular system requirement. Notice that there is only a very small overshoot on start-up, even at the rather light load of 150W. Figure 18 shows the inrush current at start-up. With a step input of 220V_{rms} the peak inrush current is about 6.5A. The chop output start-up is shown in Figure 19 This is also easily adjusted to meet system requirements.

Table 1. Circuit Component Values for 600W Boost-Chop Distributed Power System

Component	Reference	Value
Boost Inductor	L1	63µH , ±10% at 30ADC
Boost Diode	CR1	15A, 600V MUR1560
Boost Output Capacitor	C1	470uF, ±20%, 450V Aluminum Electrolytic
Chop Input Capacitors	C3, C4	3.3µF, ±10%, 400V Polypropylene
Chop Transformer	T1	Primary Turns: 42 Secondary Turns: 8
Chop Output Diodes	CR2	30A, 600V, FEP30JP
Chop Output Inductor	L2	70.7µH, +20%, -12% at 16ADC
Chop Output Capacitors	C4, C5, C6	14000µF, ±20%, 50V Aluminum Electrolytic

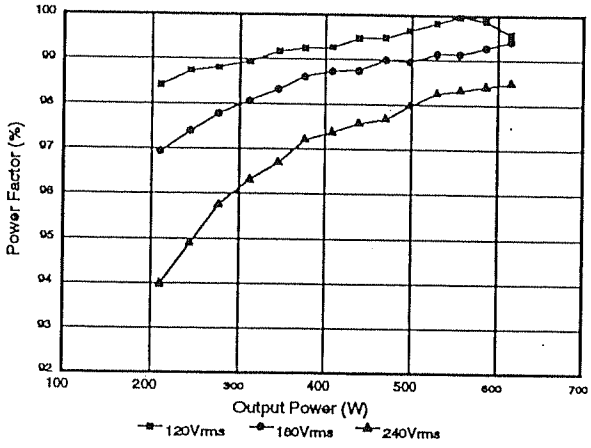

Figure 13. Power Factor

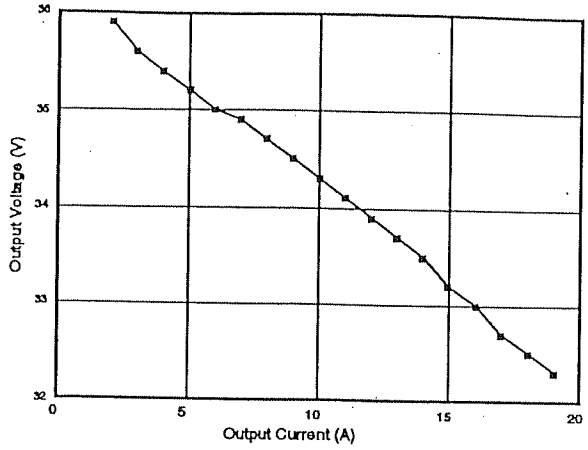

Figure 16. Output Voltage Regulation

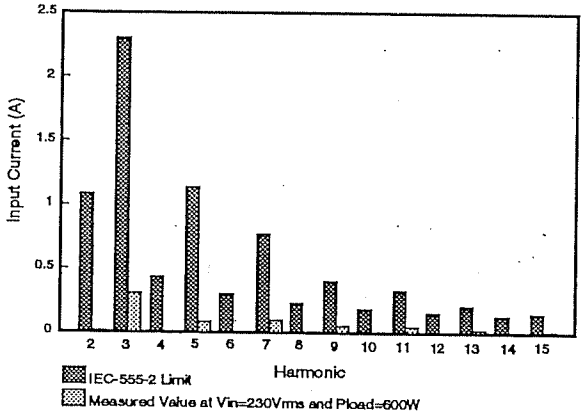

Figure 14. AC Line Current Distortion. V_{in} = 120V_{rms} and P_{load} = 600W

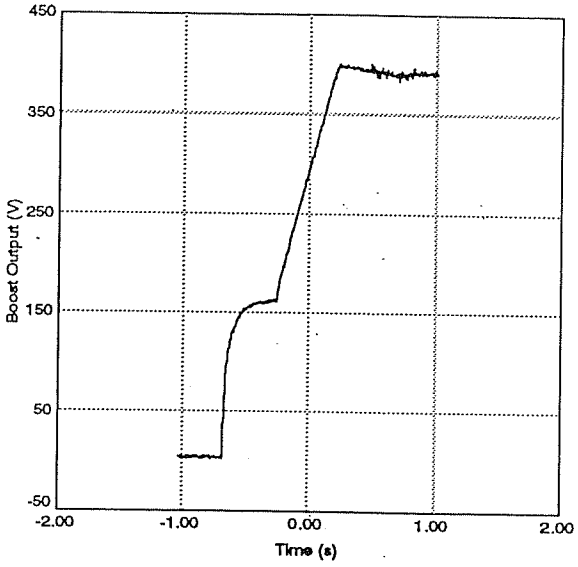

Figure 17. Boost Output Start-up. V_{in} = 120V_{rms} and P_{load} = 150W

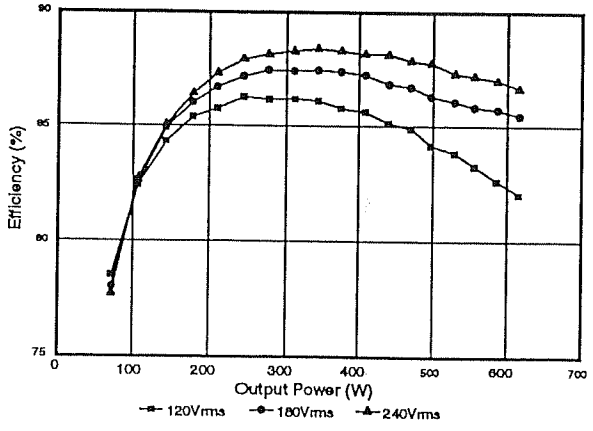

Figure 15. Efficiency

Output voltage ripple at 120Hz is less than 200mV_{p-p} even at low AC input voltage and maximum load, as shown in Figure 20. This is of course partly a function of boost and chop output capacitance. The capacitance value was chosen to allow only a 10% dip in output voltage during a 20ms drop in AC input voltage at 600W load.

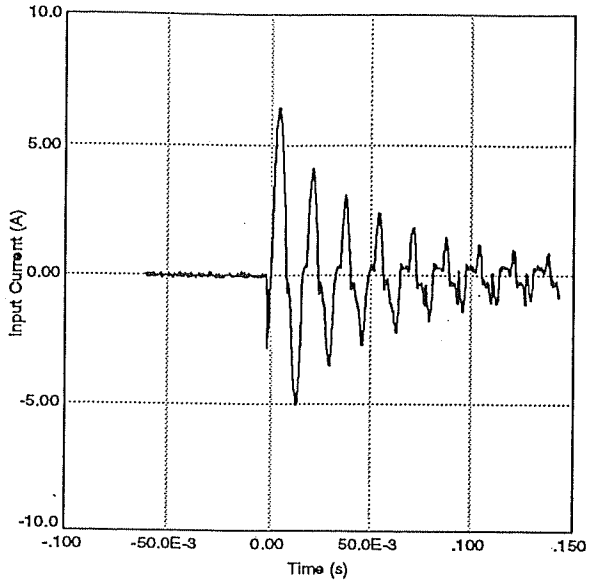

Figure 18. AC Line Inrush Current. V_{in} = $220V_{rms}$

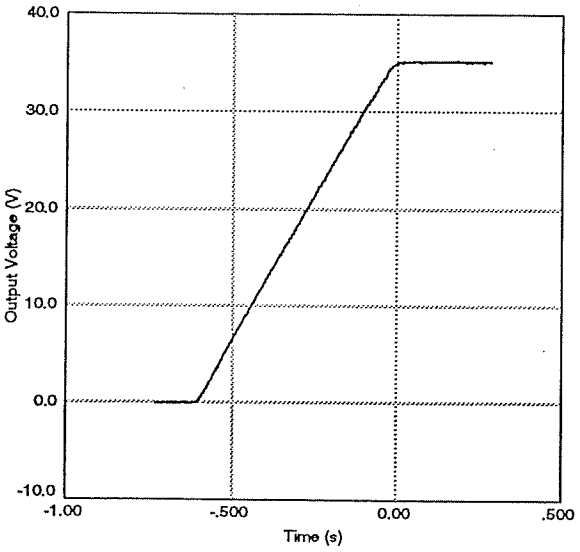

Figure 19. Chop Output Start-up. P_{load} = 100W

The output short circuit response of the chop is shown in Figure 21. The initial large current spike is due to the discharge of the chop output capacitors. However, after the initial spike, the current is limited to about 30A for about 40 ms and then the chop latches off. Both the 30A current limit value and the time before latching off are easily adjustable by changing one or two component values.

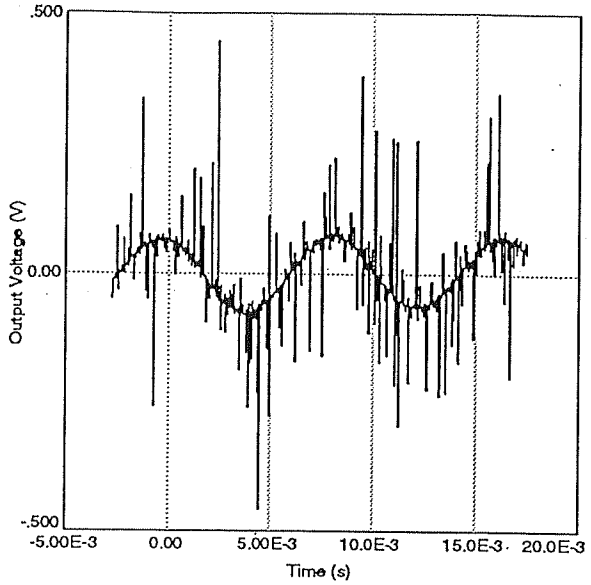

Figure 20. Output Voltage Ripple. V_{in} = $120V_{rms}$ and P_{load} = 600W

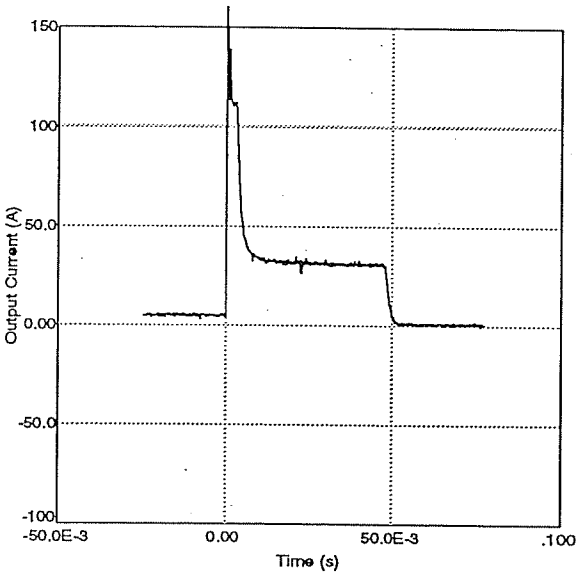

Figure 21. Output Short Circuit Current Response

Finally, the load transient dynamic response is illustrated in Figure 22 The output current is stepped between 2A and 19A. The voltage overshoots and undershoots about 1.0V beyond its steady-state values. As expected the response time is slow, because of the low bandwidth of the boost stage.

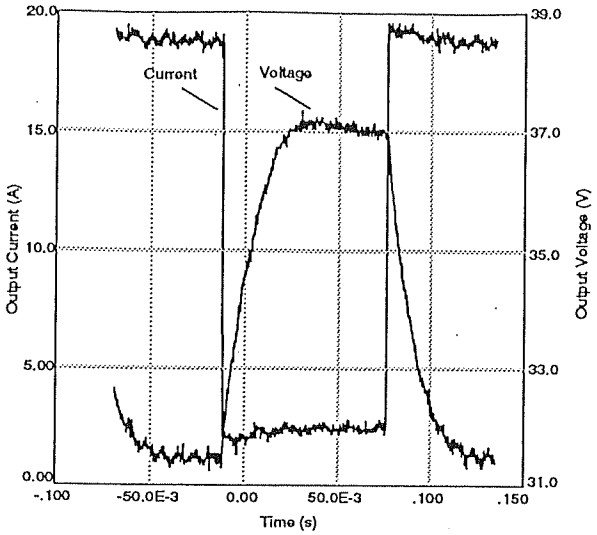

Figure 22. Output Transient Load Response. V_{in} = $120V_{rms}$

Conclusions

The cascaded zero-current switched boost and unmodulated, zero-voltage switched half-bridge or boost-chop is an appropriate topology for medium to high power distributed power systems. IEC standard 555-2 is met with margin, the system efficiency is high, and output voltage variation is only about 5% from minimum to maximum load. An inline IGBT effectively protects devices against power line disturbances. Devices are not stressed beyond manufacturers ratings. The modular, building block approach provides design flexibility and reduces manufacturing costs.

References

1. Bob Mammano and Lloyd Dixon, "Choose the Optimum Topology for High Power Factor Supplies," *PCIM*, March 1991.
2. Carlos Alberto Canesin and Ivo Barbi, "A Unity Power Factor Multiple Isolated Outputs Switching Mode Power Supply Using a Single Switch," IEEE APEC Conference, 1991.
3. K. A. Amarasinghe and C. D. Manning, "A Resonance Power Supply That Provides Dynamic Power Factor Correction in Capacitor Input Off-Line Converters," IEEE APEC Conference, 1990.
4. Herman Neufeld, "Control IC for Near Unity Power Factor In SMPS," Proceedings of PC, October 1989.
5. Neil J. Barabas, "Simplified Control Algorithm for Active Power Factor Correction," Proceedings of PCI, 1985.
6. W. A. Peterson, M. S. Elmore and S. D. Sherwood, "A Power Factor Enhancement Circuit," IEEE APEC Conference, 1991.
7. Mehmet K. Nalbant, "Design of a 1kW Power Factor Correction Circuit, "Proceedings of PC, October 1989.
8. Brad Hall, "Correct Power Factor In Switched Mode Power Supplies," *Electronic Design*, October 27, 1988.