Input Current Ripple Cancellation in Synchronized, Parallel Connected Critically Continuous Boost Converters

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Abstract - **In high power factor AC-to-DC applications boost converters operating on the boundary of continuous mode and discontinuous mode switch with variable frequency and draw high peak input currents. A method is presented to parallel two or more of these converters to reduce the high peak input currents. Each converter continues to operate on the boundary of continuous mode and discontinuous mode and maintains the benefits of zero-voltage switching.**

I. INTRODUCTION

The topology of choice for power factor correction (PFC) has been the constant frequency, continuous mode boost (CFCM). Since the boost inductor current is essentially the input current, it is easy to program the input current waveform using current mode control. Differential mode electromagnetic interference (DM-EMI) is minimized, because of the low input current ripple. Several integrated control circuits have been developed, because of these advantages [1,2].

The CFCM boost for PFC has its disadvantages, too. When the boost switch is turned on, stored charge in the boost diode must be recovered. This diode reverse recovery charge creates a large current spike that increases losses in both the switch and diode. The current spike is also a source of broadband EMI that can be difficult to manage.

Efforts to manage the limitations of the CFCM boost have produced some zero-voltage transition variations [3,4]. These techniques use a second switch to softly recover the boost diode through a small inductor at the end of each off-time. Efficiency improvements of about 1 - 2% can be expected. Commercial integrated control circuits that implement this method are also becoming available [5].

Another control technique to eliminate the disadvantages of the CFCM boost is to switch on the boundary between continuous and discontinuous inductor current (CM/DM), as shown in Fig. 1. This boundary switching is often referred to as critically continuous mode. The boost switch is programmed to turn-on, when the boost inductor current goes to zero at the end of the off-time. When the inductor current goes to zero, the voltage on the switch falls, as energy stored in the capacitance on the drain flows back to the input. By timing the boost to turn-on, when the voltage on the switch has reached a minimum value, switch turn-on losses can be significantly reduced or eliminated. Since there is no current flowing through the boost diode at turn-on, the problems associated with switching the diode are not present.

The CM/DM technique provides a highly efficient PFC circuit, but at a price. The switch peak current is twice the input peak current. This results in a higher rms switch current than with the CFCM boost, so that some of the efficiency gains due to zero-voltage turn-on are lost. A bigger problem is the larger DM-EMI, due to these very high peak inductor currents. A 900W CM/DM PFC boost, operating with 120Vrms input voltage, will have a peak inductor current in excess of 21A. It is for this reason that some investigators have concluded that the CM/DM PFC boost is not suitable for high power applications [6].

This paper shows that the CM/DM PFC boost is suitable for high power applications. If two or more CM/DM PFC boosts are paralleled and synchronized (PS), the input current ripple is reduced and the DM-EMI can be managed with a reasonably sized input filter. Several recent papers have presented circuits to parallel PFC boost converters to achieve high levels of power conversion. A technique to parallel CFCM PFC boosts is discussed in [7]. An interesting circuit to parallel hysteretically controlled PFC boosts is given in [8]. [8] hints at a small signal control method, but achieves the paralleling and synchronizing of two variable frequency PFC boosts by coupling the boost inductors.

A closed-loop small signal technique is presented here. In

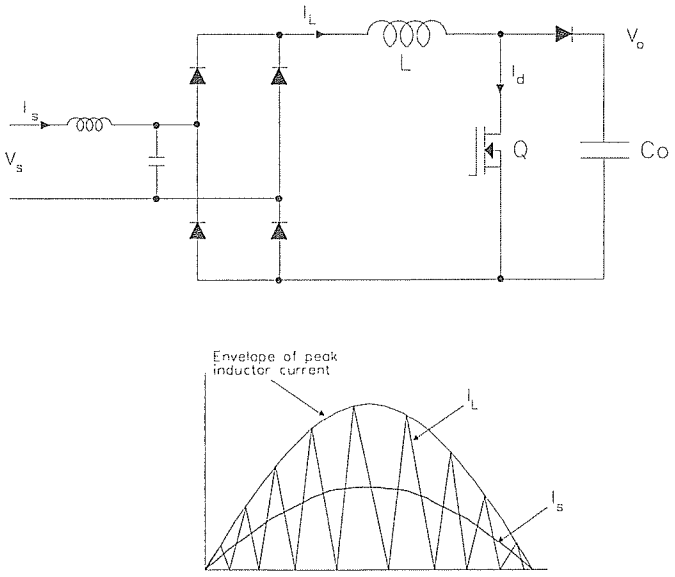

Fig. 1 - Boost Converter Operating on the Boundary Between Continuous and Discontinuous Mode

section II the control for the CM/DM PFC is summarized. In section III a circuit is presented to parallel and synchronize two or more CM/DM PFC boosts. The input rms currents are calculated and compared to the unsynchronized case in section IV. A small signal analysis is developed in section V. And finally in section VI, a design example of two PS-CM/DM PFC boosts delivering 1800W is given.

II. The CM/DM PFC Boost

The control for the CM/DM PFC boost presented in this paper is shown in Fig. 2. During the switch on-time the input voltage, V_s is dropped across the inductor and inductor current, I_L increases linearly. The control maintains a constant on-time throughout a 120Hz half-cycle of the input voltage. The voltage loop bandwidth is about 15Hz. The low bandwidth prevents boost output ripple from contributing to input current distortion. The control uses a feedforward circuit to correct for changes in loop gain with changes in line voltage. The output of SQRT is a current given by

$$Ie = \frac{k_1\sqrt{Vcomp}}{Inrms}, \qquad (1)$$

where k_1 is a constant. The output of SQRT is loaded with resistor R_e, so that $V_e = I_e R_e$. CAPCUR converts V_e to a charging current for timing capacitor C_t. The output of CAPCUR is

$$I_{c_t} = \frac{k_2}{V_e}, \qquad (2)$$

where k_2 is a constant. When the voltage on C_t reaches V_e, the comparator changes state and turns off the main switch FET. At the same time C_t is discharged to two diode drops above ground and remains discharged until the end of the off-time.

During the off-time the voltage across the inductor of Fig. 1 is monitored. When the inductor fully discharges into the output capacitor and load, the voltage on the drain of the FET starts to fall. The drain voltage is allowed to fall to a minimum value and then the FET is turned on. The control portion for turn-on is not illustrated, but Gate in Fig. 2 is brought low to allow C_t to start charging.

Normally, V_e would change in response to a change in line or load to maintain a constant output voltage. The small signal response would will be invariant with line and load, because of the feedforward circuit.

III. The PS-CM/DM PFC Boost

It was mentioned in the introduction that the CM/DM PFC boost is generally considered to be unsuitable for high power applications. In fact to deliver 1800W at an input voltage of

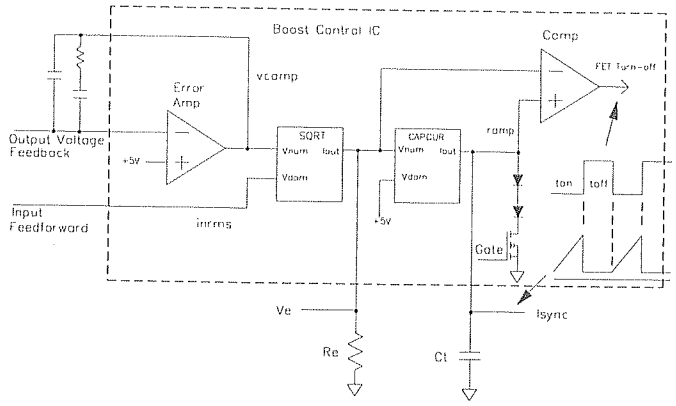

Fig. 2 - Modulator and Output Regulation Error Amplifier for the CM/DM PFC Boost

120Vrms an inductor current in excess of 42A is required. Fig. 3 shows the inductor current of a CM/DM PFC boost at a load of 1800W. The current looks solid, because of the large number of switch cycles. At an input voltage of 90Vrms the peak current would be more than 56A. This is unacceptable, on account of the high stresses on the switch FET and output diode. Also, the DM-EMI would result in a very large input filter.

Fig. 4 shows the PS-CM/DM PFC. The inputs of two boosts are common at the input capacitor on the DC side of the input rectifier. The outputs are joined at the cathodes of the boost diodes. To force current sharing the outputs of the SQRT circuits of each boost are joined. This makes a common V_e for the two boosts. When not paralleled, V_e of one boost is higher than V_e of the other, because of component variations in the output voltage regulation loops. If the two boosts did not share a common V_e, the boost with the lower unparalleled V_e would shut down. When paralleled, the higher V_e becomes the V_e for both boosts. The common V_e, however, only forces the two boosts to share current in roughly equal proportions. The common V_e does not necessarily reduce the peak input current, which is a sum of the individual inductor currents. In fact, unless something is done to properly align the individual inductor currents, they could randomly add and give a peak input current equal to twice the individual inductor currents, as shown in Fig. 3. The switching of the individual FETs must be

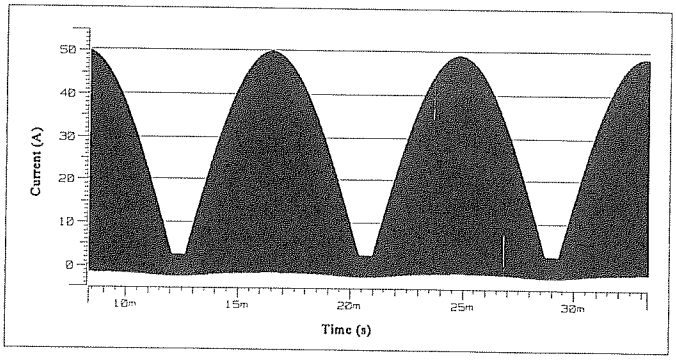

Fig. 3 - Combined Inductor Currents of non-PS-CM/DM PFC Boosts at V_s = 120Vrms and P_o = 1800W.

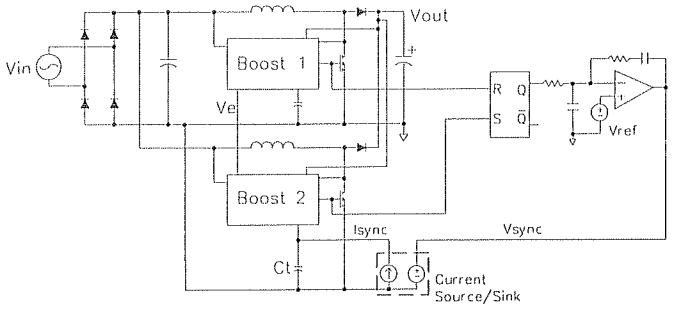

Fig. 4 - Block Diagram of the PS-CM/DM PFC Boost

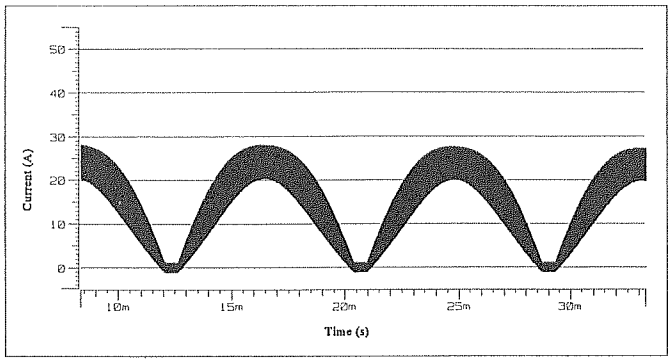

Fig. 5 - Combined Inductor Current of PS-CM/DM PFC Boost

synchronized.

To accomplish the synchronization the FET gate drives of boost 1 and boost 2 are tied to the inputs of an RS flip-flop. The output of the RS flip-flop is smoothed with a lowpass filter and becomes the input to a stabilizing error amplifier. The output of the error amplifier is converted to sink or source current that is used to adjust the charging current in the timing capacitor, C_t of boost 2. By adding or removing current from C_t, the frequency of boost 2 can be changed to synchronize its switching to boost 1. By properly selecting the reference of the error amplifier, the synchronization can be optimized to minimize the input current ripple. Fig. 5 shows the combined inductor current of the PS-CM/DM PFC boost at a load of 1800W and an input voltage of 120Vrms.

The circuit to sink or source current from C_t of boost 2 is given in Fig. 6. Fig. 7 illustrates how the frequency of boost 2 is adjusted to synchronize the two boosts.

Suppose that boost 2 is operating at a higher frequency than boost 1. This is shown in the inductor currents in Fig. 7. Boost 2 is shown with a shorter turn-on time, than boost 1. Since the turn-off times are equal, boost 2 switches at a higher frequency, than boost 1. The RS flip-flop resets at the end of the turn-on time of boost 1 and sets at the end of the turn-on time of boost 2. The RS flip-flop output is shown at the top of Fig. 7. The output switches between 0V and 5V. Since the output averages to a low value at the beginning of the switching pattern, V_{sync} in Fig. 6 is greater than 2.5V, because of the inversion of the error amplifier. This causes I_{sync} to sink current coming from CAPCUR in Fig. 2 and C_t charges more slowly. The frequency of boost 2 decreases.

On the other hand if boost 2 is switching at a lower frequency than boost 1, then the output averages to a high value at the beginning of the switching pattern. V_{sync} is less than 2.5V and I_{sync} sources current into C_t to augment the current from CAPCUR. This causes C_t to charge more quickly and the frequency of boost 1 increases.

Once the two boosts are in phase, V_{sync} attains a steady-state value, which is not necessarily 2.5V. The value of V_{sync} could differ slightly from 2.5V, because of component value variations, especially in the boost inductors. The instantaneous frequency of operation of a single boost is given by

$$f(t)=\frac{V_o-V_s(t)}{T_{on}V_o}, \tag{3}$$

where $V_s(t)$ is the instantaneous input voltage and V_o is the output voltage. T_{on} is a function of the boost inductor and is expressed as

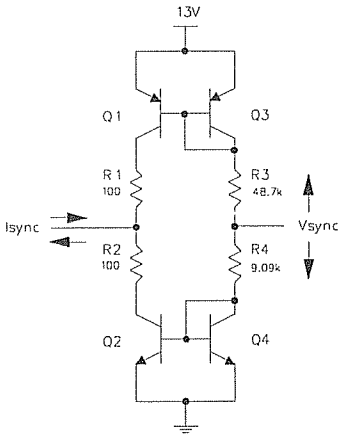

Fig. 6 - Voltage Controlled Current Source/Sink

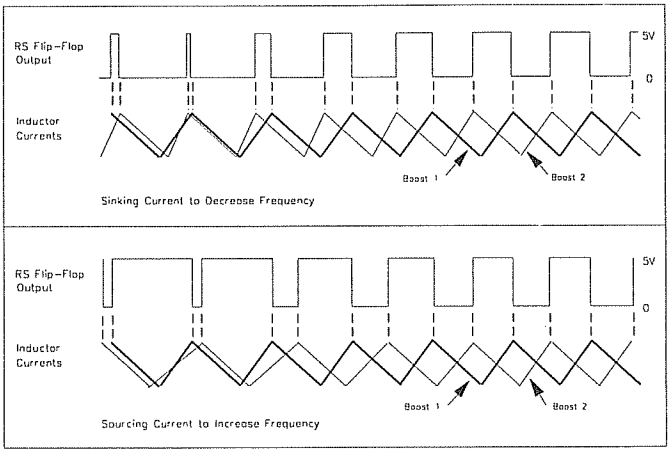

Fig. 7 - Increasing or Decreasing the Boost 2 Frequency by Sourcing or Sinking Current into C_t

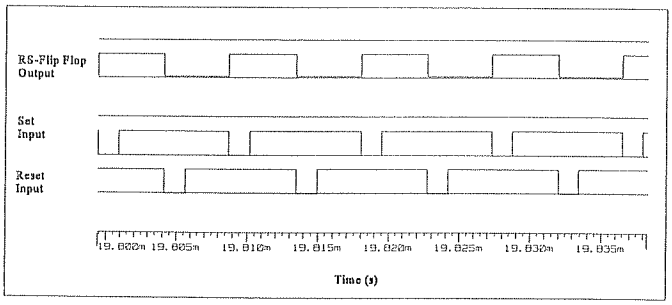

Fig. 8 - RS-Flip Flop Inputs and Outputs for the Steady-State PS-CM/DM PFC Boost

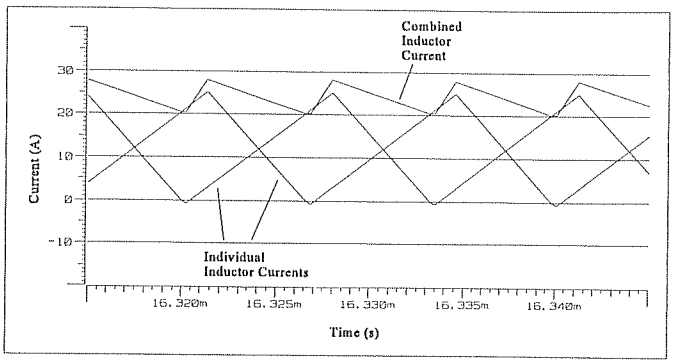

Fig. 9 - Inductor Currents of the PS-CM/DM PFC Boost

$$T_{on} = \frac{LI_{pk}(t)}{V_s(t)} = \frac{2P_s L}{V_{s_{rms}}^2}, \tag{4}$$

where P_s is the input power of the boost. The frequency of each boost will naturally vary, because of differences in the values of the inductors. So, in the steady-state V_{sync} will attain whatever value is necessary to keep boost 2 in synchronization with boost 1.

Fig. 8 shows the steady-state inputs and outputs of the RS flip-flop for a portion of the 120Hz cycle of the combined inductor current of Fig. 5.

IV. ANALYTICAL RESULTS

A. Ripple Current Analysis

The combined inductor current near the peak of the input voltage is shown in Fig. 9. An expression for the peak-to-peak value of the combined inductor current can be derived in terms of the individual inductor currents.

Some observations simplify the analysis:

1) The period of the combined ripple current is one-half the period of the individual inductor currents.

2) The off-time, $T'_{off}(t)$ of the combined inductor current is equal to the off-time, $T_{off}(t)$ of the individual inductor currents.

3) Or the on-time, $T'_{on}(t)$ of the combined inductor current is equal to the on-time, T_{on} of the individual inductor currents.

Observations two and three require that the analysis is done for two cases. $T'_{off}(t) = T_{off}(t)$ iff $T_{off}(t) < T_{on}$ and $T'_{on}(t) = T_{on}$ iff $T_{on} < T_{off}(t)$. Only the case shown in Fig. 9 for $T_{off}(t) < T_{on}$ will be analyzed here. The analysis for the other case is similar. Just the result will be given.

Inspection of Fig. 9 shows that during $T'_{on}(t)$ the slope, $m'(t)$ of the combined inductor current is the sum of the slopes, $m(t)$ of the individual inductor currents. Since the peak of the individual inductor current is $I_{pk}(t)$,

$$m'(t) = \frac{2I_{pk}(t)}{T_{on}}. \tag{5}$$

Since $T'_{off}(t) = T_{off}(t)$ in this case,

$$T'_{on}(t) = \frac{T_{on} - T_{off}(t)}{2} \tag{6}$$

by applying observation one.

From (5) and (6) come

$$I'_{pk}(t) = I_{pk}(t)\frac{T_{on} - T_{off}(t)}{T_{on}}. \tag{7}$$

(7) can be expressed in terms of circuit parameters of the individual CM/DM PFC circuit. It can be shown that for the individual circuit

$$T_{off}(t) = \frac{LI_{pk}(t)}{V_o - V_s(t)}. \tag{8}$$

If (4) and (8) are substituted into (7), the result is

$$I'_{pk}(t) = \frac{2P_s}{V_{s_{rms}}^2} V_s(t)\left[1 - \frac{V_s(t)}{V_o - V_s(t)}\right]. \tag{9}$$

The combined peak current is a function of time, because the combined peak current varies within the half-cycle of line voltage, just as the individual currents do. The worse case combined peak current is found when $V_s(t) = \sqrt{2}V_{s_{rms}}$. In this

case

$$I'_{pk_{max}} = \frac{2\sqrt{2}P_s}{V_{s_{rms}}}[1 - \frac{\sqrt{2}V_{s_{rms}}}{V_o - \sqrt{2}V_{s_{rms}}}]. \quad (10)$$

The case for $T_{on}(t) < T_{off}(t)$ produces $-I'_{pk}(t)$, so that in general the magnitudes of (9) and (10) give the peak-to-peak ripple of the combined inductor current.

The rms value of the instantaneous combined inductor current is just

$$I'_{rms}(t) = \frac{I'_{pk}(t)}{\sqrt{3}}. \quad (11)$$

The instantaneous frequency is found from (3) and (4) and the second observation. It is

$$f'(t) = \frac{V^2_{s_{rms}}}{P_s L}[\frac{V_o - V_s(t)}{V_o}]. \quad (12)$$

B. DM-EMC Filter Design

One possible filter along with the termination of the artificial mains network is shown in Fig. 10. The input ripple current of the PS-CM/DM PFC is modeled as a current source. L_1 and L_2 are DM inductors, whereas L_3 is the CM inductor leakage. C_1 is a polypropylene capacitor on the DC side of the input rectifier. C_2 and C_3 are X-capacitors. R is the 50Ω artificial mains termination.

The magnitude of the fundamental frequency component of the combined DM-EMI current can be approximated by the high frequency rms line current given in (11) [7]. As a practical matter only the worse case rms current is considered. For example, with V_s = 120Vrms and P_s = 900W $I'_{rms_{max}}$ = 3.22A. This is less ripple than is shown in Fig. 9, which depicts the same line and load conditions. The reason is that (11) and (12) do not include an efficiency term. Also, the resonant action of the FET drain capacitance and boost inductor at turn-off increase the effective on-time slightly. Nevertheless, (11) is a good approximation, since it errs on the high side.

From (12) the minimum frequency of the PS boost is 184kHz with L = 50μH. To comply with the VDE 0871, Class B requirements the EMI voltage across the artificial mains network must be 55dBμV at 184kHz.

If C_1 = 3.3μF, C_2 = 2.0μF, C_1 = 1.0μF, L_1 = L_2 = 34μH and L_3 = 9μH, the EMI voltage at 184kHz across the 50Ω is 52dBμV.

V. SMALL SIGNAL ANALYSIS

The small signal behavior was modeled with Simplis and is presented in Fig. 11. The compensation network is designed to give about 90 degrees of phase shift with a bandwidth of 2kHz. There is a trade-off between increasing bandwidth and noise sensitivity in the phase detector of Fig. 4. Care must be taken in the layout of the entire circuit to minimize noise induced phase jitter.

VI. EXPERIMENTAL RESULTS

A 1800W prototype PS-CM/DM PFC boost has been built. This boost is part of a two board system that delivers 5.2V at 200A, +12V at 35A, -12V at 3A and +24V at 8A. The total output power is limited at any time to 1200W. The power density of the boost converter and EMC filter is about 16W/in^3. The input voltage range is 85Vrms to 264Vrms. The final assembly meets VDE 0871, Class B with 6dB margin.

Fig. 12 shows the prototype. Two 900W CM/DM PFC boost modules are mounted on a motherboard that also contains the EMC filter, bias supply and small synchronizing control card. A single 900W boost module is shown in Fig. 13. The bias supply is a flyback converter that operates from the boost output. The synchronizing control is split between the boost modules and the control card. To minimize noise problems the voltage controlled sink/source circuit is located on the boost module near its timing capacitor, C_t. The RS-flip-flop is located on the control card.

A 74HC4046A with positive edge triggering implements the RS flip-flop portion of the synchronization circuit. The gate

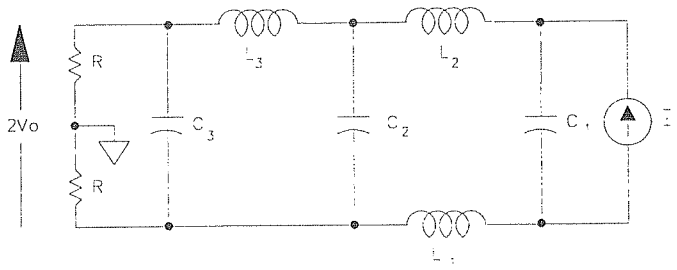

Fig. 10 - EMC Filter for the 1800W PS-CM/DM PFC Boost

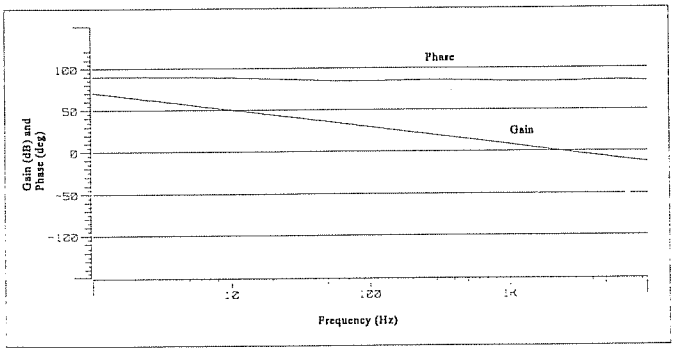

Fig. 11 - Frequency Response of the PS-CM/DM PFC Boost Phase Control

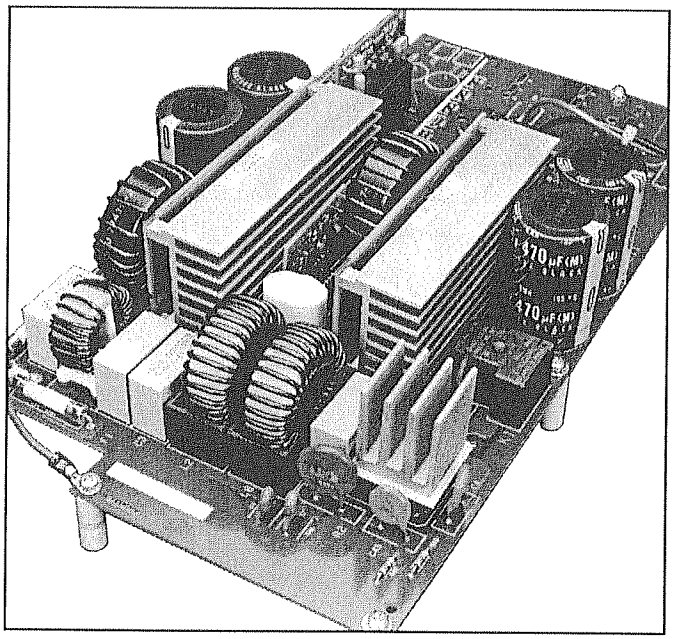

Fig. 12 - Breadboard of the 1800W PS-CM/DM PFC Boost

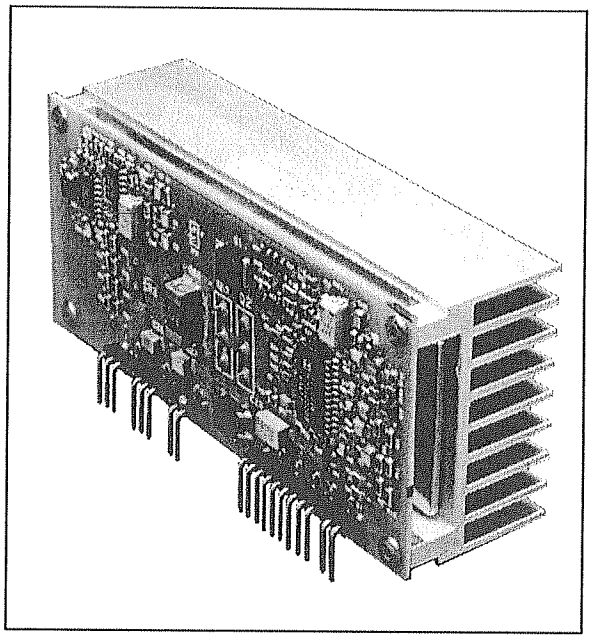

Fig. 13 - A 900W Universal Input CM/DM PFC Boost

drives from each boost are divided down to TTL levels and buffered with hex inverters. The hex inverters also give the proper phasing for the control.

Fig. 14 shows the sum of the two inductor currents and Fig. 15 shows the input current and voltage at V_s = 120Vrms and P_o = 1800W. The ripple and input currents are higher than the computer simulation given in Fig. 5, because of non-linearity in the boost inductors. Fig. 16 shows the power factor and Fig. 17 shows the efficiency. The efficiency data includes the contributions of the EMC filter losses and the bias supply.

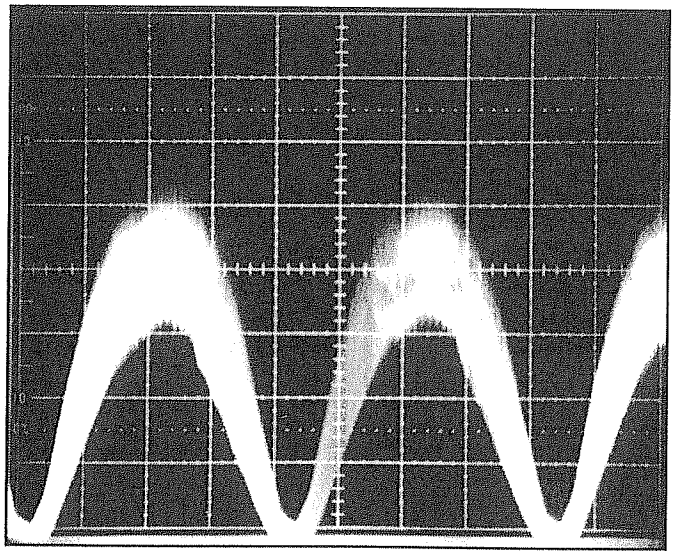

Fig. 14 - Combined Inductor Currents of the 1800W PS-CM/DM PFC Boost Operating at a 120Vrms Input Voltage (Vertical - 10A/div, Horizontal - 2ms/div)

VII. CONCLUSIONS

It has been demonstrated that a high power CM/DM PFC boost is practical. Input ripple current can be reduced to a level that is easily managed with a modestly sized DM-EMC filter. This paralleling technique is appealing, because it utilizes lower power CM/DM PFC building blocks, as shown in Fig. 13. Modules can be used individually in lower power applications and then paralleled in higher power applications. This drives the number of modules used to a higher volume and reduces cost.

It is possible to parallel more than two CM/DM PFC boost converters for either higher power applications or to reduce the

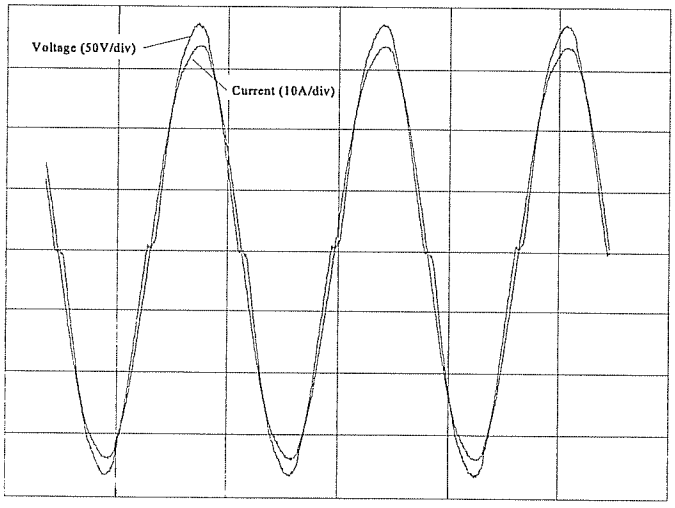

Fig. 15 - Input Current and Ripple of the 1800W PS-CM/DM PFC Boost Operating at a 120Vrms Input Voltage (Horizontal - 10ms/div)

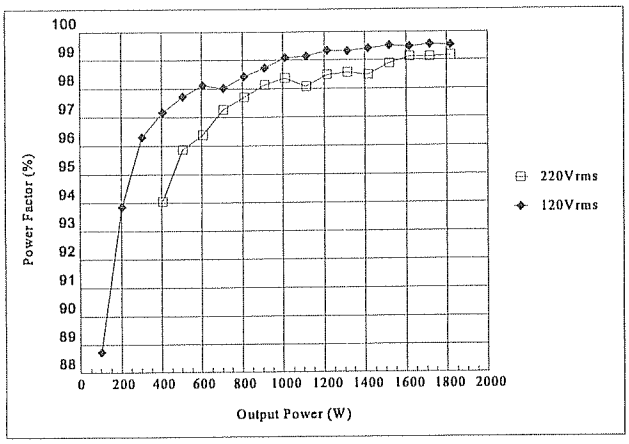

Fig. 16 - Power Factor of the PS-CM/DM PFC Boost

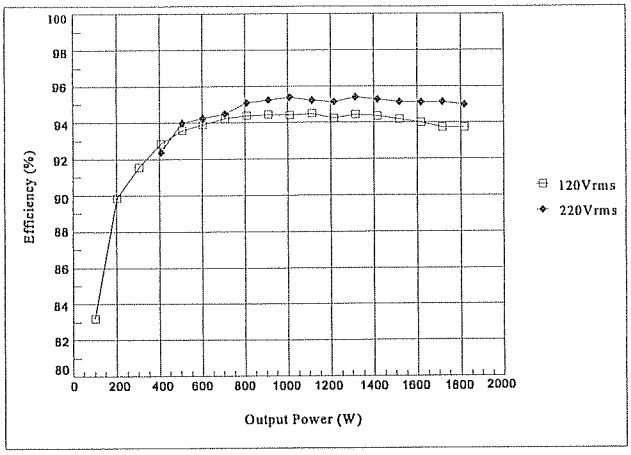

Fig. 17 - Efficiency of the PS-CM/DM PFC Boost
The efficiency data includes the input EMC filter and a small flyback bias supply

input current ripple further. Two control circuits can be used to phase the switching of a second and third boost 120 and 240 degrees with respect to the first boost. Furthermore, this technique is not restricted to CM/DM boosts, but can be applied to CM boosts. The technique has even been used with variable frequency, zero-voltage switched buck converters.

An analysis of the output current ripple and an analytical model of the small signal response still need to be developed.

ACKNOWLEDGMENT

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